Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-5 (Canceled)

6. (Currently Amended) A semiconductor device comprising:

a memory circuit provided in a semiconductor substrate; and

a test circuit ~~testing~~ that tests said memory circuit in a test mode and is incorporated into said semiconductor substrate together with said memory circuit, said test circuit comprising:

a test pattern register storing a test pattern data, said test pattern data being written in said memory circuit in said test mode;

an address register storing an address data, said test pattern data being written in an address of said memory circuit indicated by said address data; and

a first external terminal shared to receive serially said test pattern data and said address data.

7. (Previously Presented) The semiconductor device according to claim 6, wherein said test circuit further comprises:

a selection register storing a selection data, said selection data indicating which of said test pattern register and said address register receives data from said first external terminal.

8. (Previously Presented) The semiconductor device according to claim 7, wherein said first external terminal is shared to receive serially said selection data.

9. (Previously Presented) The semiconductor device according to claim 6, wherein said test circuit further comprises:

an addressing register storing an addressing mode data, said addressing mode data indicating how said memory circuit is addressed to write said test pattern data.

10. (Previously Presented) The semiconductor device according to claim 9, wherein said addressing mode data indicates whether said address data is incremented or decremented.

11. (Previously Presented) The semiconductor device according to claim 9, wherein said first external terminal is shared to receive said addressing mode data.

12. (Previously Presented) The semiconductor device according to claim 6, wherein

said test mode has a test setting mode and a test executing mode,

in said test setting mode, said test pattern register and said address register receive said test pattern data and said address data respectively,

in said test executing mode, said test pattern register and said address register output data stored therein to said memory device,

said test setting mode is conducted when a test control signal input from a second external terminal has one logic state, and

said test executing mode is conducted when said test control signal has another logic state.

13. (Previously Presented) The semiconductor device according to claim 6, wherein said test circuit further comprises a reverse circuit outputting data in which the value of said test pattern data is reversed.

14. (Previously Presented) The semiconductor device according to claim 6, wherein said test pattern register and said address register are shift registers.

15. (Currently Amended) A semiconductor device comprising:

a memory circuit provided in a semiconductor substrate; and

a test circuit that tests said memory circuit in a test mode and is incorporated into said semiconductor substrate together with said memory circuit, said test circuit comprising:

a test pattern register storing a test pattern data, said test pattern data being written in said memory circuit[[:]];

a selection register storing a selection data, said selection data indicating whether said test pattern register is selected to receive said test pattern data; and

a first external terminal shared to receive serially said test pattern data and said selection data.

16. (Previously Presented) The semiconductor device according to claim 15, wherein said test circuit further comprises an addressing register storing an addressing mode data, said addressing mode data indicating how said memory circuit is addressed to write said test pattern data.

17. (Previously Presented) The semiconductor device according to claim 16, wherein said addressing mode data indicates whether said address data is incremented or decremented.

18. (Previously Presented) The semiconductor device according to claim 7, further comprising a second external terminal receiving a setting mode data,

wherein said test pattern register or said address register receives said test pattern data or said address data respectively from said first external terminal when said setting mode data has one logic state, and

said selection register receives said selection data from said first external terminal when said setting mode data has another logic state.

19. (Currently Amended) The semiconductor device according to claim 15, further comprising a second external terminal receiving a setting mode data,

wherein said test pattern register ~~deceives~~ receives said test pattern data from said first external terminal, and

said selection register receives said selection data from said first external terminal when said setting mode data has another logic state.